M.E. (VLSI DESIGN - REGULAR)

CURRICULUM AND SYLLABI 2015
(REGULAR PROGRAMME)

Department of Electronics and Communication Engineering
FACULTY OF ENGINEERING

KARPAGAM ACADEMY OF HIGHER EDUCATION
(Established Under Section 3 of UGC Act 1956)
Eachanari post, COIMBATORE 641 021, INDIA
SEMESTER - I

15MECC101  APPLIED MATHEMATICS  3 1 0 4 100

OBJECTIVES:

<table>
<thead>
<tr>
<th>To teach the fundamental concepts of integral equations and mathematical modeling of the problems</th>
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<tr>
<td>To study about Calculus of variations and Random Process</td>
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<td>To teach transforms and its applications</td>
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OUTCOMES:

- Acquires the knowledge of special functions and applications of modelling
- Able to solve ordinary faction numerically.

UNIT - I  UNIT – I  INTEGRAL EQUATIONS

UNIT - II  CALCULUS OF VARIATIONS
Variation and its properties – Euler’s equation – Functional dependent on first and higher order derivatives – Functional dependent on functions of several independent variables – Some applications – Direct methods: Ritz and Kantorovich methods.

UNIT - III  LINEAR PROGRAMMING
Basic concepts – Graphical and Simplex methods – Transportation problem – Assignment problem.

UNIT – IV  Z – TRANSFORMS

UNIT – V  RANDOM PROCESSES

TEXT BOOKS:

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<tr>
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<tr>
<td>2</td>
<td>Gupta.A.S.</td>
<td>Calculus of Variations with Applications</td>
<td>Prentice Hall of India, New Delhi</td>
<td>1999</td>
</tr>
</tbody>
</table>

WEBSITES:

1. www.phpsimplex.com
2. www.mathyards.com
3. www.mathworld.com
OBJECTIVE:
1. To introduce methods to analyze and design synchronous and asynchronous sequential circuits
2. To introduce variable entered maps and techniques to simplify the Boolean expressions using these maps
3. To explain the design procedures for developing complex system controllers using digital ICs

OUTCOMES:
1. Ability to analyze and design sequential digital circuits
2. Ability to understand the requirements and specifications of the system required for a given application
3. Decide a suitable system controller architecture
4. Design system controllers using different digital ICs

UNIT I  SEQUENTIAL CIRCUIT DESIGN
Analysis of Clocked Synchronous Sequential Networks (CSSN) Modeling of CSSN – State
Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits – ASM Chart –
ASM Realization.

UNIT II  ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN
Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC –
State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic
Hazards – Essential Hazards – Data Synchronizers – Designing Vending Machine Controller –
Mixed Operating Mode Asynchronous Circuits.

UNIT III  FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS
Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi
Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA’s – Fault in PLA –
Test Generation – Masking Cycle – DFT Schemes – Built-in Self Test

UNIT IV  SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES
EPROM to Realize a Sequential Circuit – Programmable Logic Devices – Designing a
Synchronous Sequential Circuit using a GAL – EPROM – Realization State machine using PLD –
FPGA – Xilinx FPGA – Xilinx 2000 - Xilinx 3000

UNIT V  SYSTEM DESIGN USING VHDL
VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and
Simulation of VHDL Code – Modeling using VHDL – Flip Flops – Registers – Counters –
Sequential Machine – Combinational Logic Circuits - VHDL Code for – Serial Adder, Binary
Multiplier – Binary Divider – complete Sequential Systems – Design of a Simple
Microprocessor.

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<td>Digital principles and Design</td>
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<td>2</td>
<td>John M Yarbrough</td>
<td>Digital Logic applications and Design</td>
<td>Thomson Learning, United Kingdom</td>
<td>2001</td>
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<td>3</td>
<td>Charles H. Jr. Roth</td>
<td>Digital System Design using VHDL</td>
<td>Thomson Learning, United Kingdom</td>
<td>1998</td>
</tr>
</tbody>
</table>
OBJECTIVES:
1. To understand the concepts of MOS transistors operations and their AC, DC characteristics.
2. To know the fabrication process of cmos technology and its layout design rules
3. To understand the latch up problem in cmos circuits.
4. To study the concepts of cmos invertors and their sizing methods.
5. To know the concepts of power estimation and delay calculations in CMOS circuits.

OUTCOMES:
1. The student will understand the fundamentals of CMOS Technology.
2. The student will show the skills of designing digital VLSI.
3. The student will demonstrate the ability for using backend tools in IC technology

UNIT I VLSI DESIGN PROCESS & MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY

UNIT II INVERTERS AND LOGIC GATES
NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics, switching times, Super buffers, Driving large capacitance loads, CMOS logic structures, Transmission gates, Static CMOS design, Dynamic CMOS design.

UNIT III CIRCUIT CHARACTERISATION & PERFORMANCE ESTIMATION
Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining, Charge sharing, Scaling.

UNIT IV VLSI SYSTEM COMPONENTS CIRCUITS
Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers

UNIT V VERILOG HARDWARE DESCRIPTION LANGUAGE
Overview of digital design with Verilog HDL, hierarchical Modeling concepts, modules and port definitions, gate level Modeling, data flow Modeling, behavioral Modeling, task & functions, Test Bench.

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<td>John P.Uyemura</td>
<td>Introduction to VLSI Circuits and Systems</td>
<td>John Wiley &amp; Sons, Inc</td>
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<td>3</td>
<td>Samir Palnitkar</td>
<td>Verilog HDL</td>
<td>Pearson Education, New Delhi</td>
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OBJECTIVE:
1. To acquaint the students with fundamentals of building device and circuit simulators, and efficient use of simulators.

OUTCOMES:
1. The student who completes this course will be in a position understand the procedures used to construct the complicated device models that are widely used in VLSI CAD tools.
2. As the CMOS technology progresses, the student will be in a position to understand the changes introduced in the device models as well as contribute to the development of appropriate device models.

UNIT I BASIC SEMICONDUCTOR PHYSICS
Quantum Mechanical Concepts, Carrier Concentration, Transport Equation, Band gap, Mobility and Resistivity, Carrier Generation and Recombination, Avalanche Process, Noise Sources. Diodes: Forward and Reverse biased junctions – Reverse bias breakdown – Transient and AC conditions - Static and Dynamic behavior- Small and Large signal models – SPICE model for a Diode – Temperature and Area effects on Diode Model Parameters.

UNIT II BIPOLAR DEVICE MODELING

UNIT III MOSFET MODELING
MOS Transistor – NMOS, PMOS – MOS Device equations - Threshold Voltage – Second order effects - Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE.

UNIT IV PARAMETER MEASUREMENT

UNIT V OPTOELECTRONIC DEVICE MODELING
Static and Dynamic Models, Rate Equations, Numerical Technique, Equivalent Circuits, Modeling of LEDs, Laser Diode and Photo detectors.

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<td>Semiconductor Devices - Physics and Technology</td>
<td>John Wiley and sons</td>
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OBJECTIVES:
1. In the VLSI design industry, a significant portion of work force and resources are being deployed in the test and validation of VLSI designs. The complexity of multimillion transistor based VLSI design calls for special techniques for efficiently testing and validating the VLSI design across all possible input, supply, speed and process corners.
2. The present course will introduce the student to the mathematical and scientific principles based on which systematic test and validation can be carried out on multimillion transistor VLSI design.

OUTCOMES:
1. The student who completes this course will be familiar with the principles used in the construction VLSI Design For Test (DFT) tools.
2. The student will be able to adapt these to his specific industrial needs, also contribute to the development of more efficient tools from the fault overage and speed point of view.

UNIT I  INTRODUCTION

UNIT II  TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS
Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits.

UNIT III  DESIGN FOR TESTABILITY
Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design - System level DFT approaches.

UNIT IV  BUILT-IN SELF TEST
Built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs

UNIT V  SELF-CHECKING AND SYSTEM LEVEL DIAGNOSIS
Logic Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.

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15MEVA*51  VALUE ADDED COURSE – I

PRACTICALS

15MEVL111  VLSI DESIGN LAB I

LIST OF EXPERIMENTS
1. Modeling of Sequential Digital system using VHDL.
3. Writing Test Benches Using Verilog / VHDL
4. Design and Implementation of ALU using FPGA.
5. Simulation of NMOS and CMOS circuits using SPICE.
6. Design of Static and Dynamic Logic Circuits
7. Modeling of MOSFET using C.
8. Implementation of FFT, Digital Filters.
10. Implementation of MAC Unit using FPGA.
SEMESTER – II

15MEVL201 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS 3 0 0 3 100

OBJECTIVE:
1. To design the single stage amplifiers using pmos and nmos driver circuits with different loads.
2. To analyze high frequency concepts of single stage amplifiers and noise characteristics associated with differential amplifiers.
3. To study the different types of current mirrors and to know the concepts of voltage and current reference circuits.

OUTCOMES:
1. Student will able to do analyze characteristics of various analog devices.

UNIT I MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES

UNIT II CIRCUIT CONFIGURATION FOR LINEAR IC
Current sources, Analysis of difference amplifiers with active load using BJT and FET, supply and temperature independent biasing techniques, voltage references. Output stages: Emitter follower, source follower and Push pull output stages.

UNIT III OPERATIONAL AMPLIFIERS
Analysis of operational amplifiers circuit, slew rate model and high frequency analysis, Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise

UNIT IV ANALOG MULTIPLIER AND PLL
Analysis of four quadrant and variable Transconductance multiplier, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits: Sources of noise- Noise models of Integrated-circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY
MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic-Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers

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<td>Gray, Meyer, Lewis, Hurst</td>
<td>Analysis and design of Analog IC’s</td>
<td>Wiley International</td>
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<td>Behzad Razavi</td>
<td>Design of Analog CMOS Integrated Circuits</td>
<td>S.Chand and company Ltd</td>
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<td>Nandita Dasgupata, Amitava Dasgupta</td>
<td>Semiconductor Devices, Modeling and Technology</td>
<td>Prentice Hall of India Pvt. ltd</td>
<td>2004</td>
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<td>4</td>
<td>Alan B. Grebene</td>
<td>Bipolar and MOS Analog Integrated circuit design</td>
<td>John Wiley &amp; sons</td>
<td>2003</td>
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</table>
OBJECTIVES:
1. To know the sources of power consumption in CMOS circuits
2. To understand the various power reduction techniques and the power estimation methods.
3. To study the design concepts of low power circuits.

OUTCOME:
1. The student will get to know the basics and advanced techniques in low power design which is a hot topic in today’s market where the power plays major role.
2. The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

UNIT I POWER DISSIPATION IN CMOS
Sources of power dissipation – Physics of power dissipation in CMOS FET devices- Basic principle of low power design.

UNIT II POWER OPTIMIZATION
Logical level power optimization – Circuit level low power design: logic styles, transistor sizing and ordering – Circuit techniques for reducing power consumption in adders and multipliers.

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS
Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Advanced techniques: Adiabatic Computation, Asynchronous Circuits – Special techniques

UNIT IV POWER ESTIMATION AND ANALYSIS
Logic level power estimation – Simulation power analysis – Probabilistic power analysis

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER
Synthesis for low power –Behavioral level transforms- Software design for low power – Software Power Estimation – Software Power Optimization

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<td>2</td>
<td>Dimitrios Soudris, Christian Pignet, Costas Goutis</td>
<td>Designing CMOS Circuits For Low Power</td>
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<td>4</td>
<td>Chandrakasan.A.P and Broadersen.R.W</td>
<td>Low power digital CMOS design</td>
<td>Kluwer academic publishers, Boston</td>
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<td>5</td>
<td>Gary Yeap</td>
<td>Practical low power digital VLSI design</td>
<td>Kluwer academic publishers, Boston</td>
<td>1998</td>
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</table>
OBJECTIVES:
1. To familiarize the concept of DSP and DSP algorithms.
2. Introduction to Multirate systems and finite word length effects
3. To know about the basic DSP processor architectures and the synthesis of the processing elements
4. To gather an idea about the VLSI circuit layout design styles.

OUTCOMES:
1. Get to know about the Digital Signal Processing concepts and its algorithms
2. Get an idea about finite word length effects in digital filters
3. Concept behind multirate systems is understood.
4. Get familiar with the DSP processor architectures and how to perform synthesis of processing elements
5. Acquire an general idea about VLSI circuit layout design aspects

UNIT I  DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES
Standard digital signal processors, Application specific IC’s for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies

UNIT II  DIGITAL SIGNAL PROCESSING

UNIT III  DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS
FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT IV  DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES
DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

UNIT V  ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN
Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies.
# REFERENCES

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<td>4</td>
<td>Bayoumi and Magdy. A</td>
<td>VLSI Design Methodologies for Digital Signal Processing Architectures</td>
<td>BS Publications</td>
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**LIST OF EXPERIMENTS**

1. Implementation of 8 Bit ALU in FPGA / CPLD.
2. Implementation of 4 Bit Sliced processor in FPGA / CPLD.
5. Implementation of model train controller using embedded microcontroller.
6. System design using PLL.
SEMESTER III

15MECC301 RESEARCH METHODOLOGY PEDAGOGY & COMMUNICATION SKILLS 3 0 0 3 100

OBJECTIVES:
To make the student understand
  To introduce students to a number of perspectives on research and to broaden their conceptions of what research involves.
  To learn about research, design, information retrieval, problem formulation, use of statistical techniques

OUTCOMES:
The students will be able to:
  Plan, undertake, execute research projects and prepare relevant documents. Take up doctoral research in their area of interest and submit the thesis and defend the same successfully

UNIT I HIGHER EDUCATION AN INTRODUCTION
Historical perspectives, the objectives of higher education, role of higher education-social focus, curricular focus, administrative focus, drivers of change in higher education-globalization, changing demographics, structuring of employment, technological change, demand of accountability, consumerism,. Expectations by employers, rate of knowledge growth, campus demographics, concern for community. Restructuring and new patterns of decision making.

UNIT II RESEARCH PROCESSES AND METHODOLOGY

UNIT III EFFECTIVE RESEARCH SKILLS

UNIT IV TECHNIQUES OF TEACHING AND EVALUATION
Large group techniques – lecture, seminar, symposium, panel discussion-project approaches and workshop. Small Group techniques-group discussion simulation, role playing-Buzz techniques, brain storming, case discussion and assignment system approach in education. Individualized techniques-CAI Keller plan – PSI and programmed learning-methods of evaluation-self evaluation and student evaluation in higher education, question banking, diagnostic testing and remedial teaching.

UNIT V ESSENTIALS FOR EFFECTIVE COMMUNICATION IN ENGLISH
Improving Vocabulary stock-general and technical vocabulary-British and American vocabulary- homophones & homonyms, idioms and phrases-Different grammatical functions of the same word-Grammar-Tenses, Voice, reported speech, Modals, spoken English structures, formal and informal-letters, project reports, descriptions, circulars, synopsis and summary writing. Listening skills for competitive exams-Reading skills-skimming and scanning – Reading
journals, magazines and newspapers for comprehension. Practical use of English – conversation, seminars, individual speeches and group discussions. Reference skills-Using dictionary, thesaurus and encyclopedia effectively. Error shooting for better use of English.

### TEXT BOOKS

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<td>Kumar.K.H</td>
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### WEB SITES

- [www.english4engineer.com](http://www.english4engineer.com)
- [www.learn4good.com/language/engineer](http://www.learn4good.com/language/engineer)
OBJECTIVE:
1. To provide an introduction to the fundamentals of Computer-Aided Design tools for the modeling, design, analysis, test, and verification of digital Very Large Scale Integration (VLSI) systems.
2. To understand the advanced techniques for solving computer-aided design problems for a wide range of design styles.
3. To get knowledge required to design, implement, and test digital VLSI circuits.

OUTCOMES:
1. able to apply knowledge from undergraduate engineering and other disciplines to identify, formulate, solve novel advanced electronics engineering along with soft computing problems that require advanced knowledge within the field.
2. able to understand and integrate new knowledge within the field.
3. able to understand and design advanced electronics systems (Analog and Digital Systems) and conduct experiments, analyze and interpret data.
4. able to use modern engineering tools, software and equipments to analyze problems.

UNIT I
Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - general purpose methods for combinatorial optimization - Unit Size Problem, Backtracking, Branch and Bound.

UNIT II
Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms – partitioning

UNIT III
Floor planning concepts - shape functions and floor plan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV
Simulation - Gate-level Modeling and simulation - Switch-level Modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V
High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - High level transformations.

REFERENCES

<table>
<thead>
<tr>
<th>S.NO</th>
<th>Author(s) Name</th>
<th>Title of the book</th>
<th>Publisher</th>
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**SEMESTER IV**

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</tbody>
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LIST OF ELECTIVES

15MEVL_E01 AD-HOC NETWORKS 3 0 0 3 100

OBJECTIVE:

1. To study different kinds of temporary wireless networks
2. To study different routing protocols and it application

OUTCOMES:

1. To study different routing protocols used in ad hoc wireless networks.

UNIT I  WIRELESS LAN, PAN, WAN AND MAN

UNIT II  MAC, ROUTING AND MULTICAST ROUTING PROTOCOLS

UNIT III  TRANSPORT LAYER AND SECURITY PROTOCOLS

UNIT IV  ENERGY MANAGEMENT
Need, classification of battery management schemes, Transmission power management schemes, System power management schemes. Wireless Sensor Networks: Architecture, Data dissemination, Date gathering, MAC protocols, location discovery, Quality of a sensor network.

UNIT V  PERFORMANCE ANALYSIS
ABR beaconing, Performance parameters, Route-discovery time, End-to-end delay performance, Communication throughput performance, Packet loss performance, Route reconfiguration/repair time, TCP/IP based applications.

REFERENCES

<table>
<thead>
<tr>
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<td>C. Siva Ram Murthy and B.S. Manoj</td>
<td>AdHoc Wireless Networks: Architectures and protocols</td>
<td>Prentice Hall PTR</td>
<td>2004</td>
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<td>Systems</td>
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</table>
OBJECTIVE:
1. To study about the fundamentals of digital images.
2. To understand 1D and 2D image transforms.
3. To gain sound knowledge about various image processing techniques.

OUTCOMES:
1. Understand about Sampling Techniques
2. Know the design of Digital filters
3. Know different transform and various algorithms to evaluate them
4. Know different coding methods

UNIT I  DIGITAL IMAGE FUNDAMENTALS
Elements of digital image processing systems, Elements of visual perception, psycho visual model, brightness, contrast, hue, saturation, mach band effect, Color image fundamentals - RGB, HSI models, Image acquisition and sampling, Quantization, Image file formats, Two-dimensional convolution, correlation, and frequency responses.

UNIT II  IMAGE TRANSFORMS
1D DFT, 2D transforms – DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Radon, and Wavelet Transform.

UNIT III  IMAGE ENHANCEMENT AND RESTORATION
Histogram modification and specification techniques, Noise distributions, Spatial averaging, Directional Smoothing, Median, Geometric mean, Harmonic mean, Contra harmonic filters, Homomorphic filtering, Color image enhancement. Image Restoration – degradation model, Unconstrained and Constrained restoration, Inverse filtering, Wiener filtering, Geometric transformations– spatial transformations, Gray-Level interpolation,

UNIT IV  IMAGE SEGMENTATION AND RECOGNITION

UNIT V  IMAGE COMPRESSION
Need for image compression, Huffman, Run Length Encoding, Arithmetic coding, Vector Quantization, Block Truncation Coding. Transform Coding – DCT and Wavelet. Image compression standards.

REFERENCES

<table>
<thead>
<tr>
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<td>Rafael C. Gonzalez,</td>
<td>Digital Image Processing</td>
<td>Pearson Education, Inc</td>
<td>2004</td>
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<td>Richard E.Woods</td>
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<td></td>
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<td>Processing</td>
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</table>
OBJECTIVE:
1. To learn about basic genetic algorithms.
2. To introduce implementation and optimization aspects of genetic algorithms.

OUTCOMES:
Upon completion of this course, students will be able to:
1. Explain the of the principles underlying Evolutionary Computation in general and Genetic Algorithms in particular.
2. Analyze and experiment with parameter choices in the use of Evolutionary Computation

UNIT I INTRODUCTION

UNIT II GENETIC ALGORITHMS
Genetic technology: steady state algorithm - fitness scaling - inversion. Genetic programming - Genetic Algorithm in problem solving

UNIT III GENETIC ENGINEERING
Genetic Algorithm in engineering and optimization-natural evolution –Simulated annealing and Tabu search .Genetic Algorithm in scientific models and theoretical foundations.

UNIT IV IMPLEMENTATION
Implementing a Genetic Algorithm – computer implementation - low level operator and knowledge based techniques in Genetic Algorithm.

UNIT V OPTIMIZATION
Applications of Genetic based machine learning-Genetic Algorithm and parallel processors, composite laminates, constraint optimization, multilevel optimization, real life problem.

REFERENCES

<table>
<thead>
<tr>
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<td>Melanie Mitchell</td>
<td>An introduction to Genetic Algorithm</td>
<td>Prentice-Hall of India, New Delhi</td>
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<td>David.E.Golberg</td>
<td>Genetic algorithms in search, optimization and machine learning</td>
<td>Addision-Wesley, Boston</td>
<td>1999</td>
</tr>
</tbody>
</table>
OBJECTIVES:
1. To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
2. To introduce efficient design of DSP architectures suitable for VLSI

OUTCOME:
1. To be able to design architectures for DSP algorithms.
2. To be able to optimize design in terms of area, speed and power.
3. To be able to incorporate pipeline based architectures in the design.
4. To be able to carry out HDL simulation of various DSP algorithms

UNIT I INTRODUCTION TO DSP SYSTEMS
Introduction To DSP Systems - Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II RETIMING, FOLDING AND UNFOLDING
Retiming - definitions and properties Retiming techniques; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Folding – Folding transformation – Register minimizing techniques – Register minimization in folded architectures

UNIT III FAST CONVOLUTION
Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm – Wino grad Algorithm, Iterated Convolution – Cyclic Convolution; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES
Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh- Wooley carry-save multiplication tabular form and implementation, design of Lyon’s bit-serial multipliers using Horner’s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner’s rule for precision improvement.

UNIT V PROGRAMMING DIGITAL SIGNAL PROCESSORS
Synchronous, Wave and asynchronous pipelining- synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

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</table>
OBJECTIVES:
1. To study basics of biological Neural Network.
2. To study basics of artificial Neural Network
3. To study applications of ANN

OUTCOME:
. To get an adequate knowledge about neural theory

UNIT I BASIC LEARNING ALGORITHMS


UNIT II RADIAL-BASIS FUNCTION NETWORKS AND SUPPORT VECTOR MACHINES


UNIT III ATTRACTOR NEURAL NETWORKS


UNIT IV ADAPTIVE RESONANCE THEORY

UNIT – V  SELF ORGANISING MAPS


REFERENCES

<table>
<thead>
<tr>
<th>S.NO</th>
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OBJECTIVES:

1. To understand the difference between the pipeline and parallel concepts.
2. To study the various types of architectures and the importance of scalable architectures.
3. To study the various memories and optimization of memory.
4. To study modern architectures such as RISC, Super Scalar, VLIW (very large instruction word), multi-core and multi-CPU systems.

OUTCOME:

1. Able to apply knowledge from undergraduate engineering and other disciplines to identify, formulate, solve novel advanced electronics engineering along with soft computing problems that require advanced knowledge within the field.
2. Able to understand and integrate new knowledge within the field.
3. Able to understand and design advanced electronics systems (Analog and Digital Systems) and conduct experiments, analyze and interpret data.

UNIT I THEOREY OF PARALLELISM
Parallel Computer models – the state of computing, Multiprocessors and Multi computers and Multi vectors and SIMD computers, PRAM and VLSI models, Architectural development tracks, Program and network properties – Conditions of parallelism.

UNIT II PARTITIONING AND SCHEDULING

UNIT III HARDWARE TECHNOLOGIES
Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory – backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models.

UNIT IV PIPELINING AND SUPERSCALAR TECHNOLOGIES
Parallel and scalable architectures, Multiprocessor and Multicomputers, Multi vector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT V SOFTWARE AND PARALLEL PROCESSING
Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

REFERENCES

<table>
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<tr>
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<td>Parallel Computer Architecture</td>
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<td>John P. Shen</td>
<td>Modern processor design Fundamentals of super scalar processors</td>
<td>Tata McGraw Hill</td>
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<td>Sajjan G. Shiva</td>
<td>Advanced Computer Architecture</td>
<td>Taylor &amp; Francis</td>
<td>2008</td>
</tr>
</tbody>
</table>
OBJECTIVE:
1. To give an insight to the students about the significance of VHDL Programming
2. To teach the importance and architectural modeling of programmable logic devices.
3. To introduce the construction and design programming
4. To teach the basic VLSI design configurations
5. To study the Logic synthesis and simulation of digital system with PLD

OUTCOME:
1. Student will able to describe a system using VHDL.
2. To teach the basic VLSI design configuration
3. To understand the Logic synthesis and simulation of digital system with PLD

UNIT I VHDL FUNDAMENTALS

UNIT II COMPOSITE DATA TYPES & BASIC MODELING CONSTRUCTS

UNIT III SUBPROGRAMS AND PACKAGES

UNIT IV SIGNALS, COMPONENTS, CONFIGURATIONS

UNIT V ADTs AND FILES

REFERENCES

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<tr>
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<tr>
<td>3</td>
<td>James M. Lee</td>
<td>Verilog Quick start</td>
<td></td>
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</tbody>
</table>
OBJECTIVE:
1. To study the design flow of different types of ASIC.
2. To familiarize the different types of programming technologies and logic devices.
3. To gain knowledge about partitioning, floor planning, placement and routing including circuit extraction of ASIC

OUTCOMES:
1. Able to understand and integrate new knowledge within the field.
2. Able to apply advanced technical knowledge in multiple contexts
3. Able to understand and design advanced electronics systems (Analog and Digital Systems) and conducts experiments, analyze and interpret data.

UNIT I  INTRODUCTION

UNIT II  PROGRAMMABLE ASICS
Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and outputs – Clock and power inputs – Xilinx I/O blocks.

UNIT III  PROGRAMMABLE ASIC DESIGN SOFTWARE

UNIT IV  LOGIC SYNTHESIS, SIMULATION AND TESTING
Verilog and logic synthesis – VHDl and logic synthesis - Types of simulation – Boundary scan test – Fault simulation – Automatic test pattern generation.

UNIT V ASIC CONSTRUCTION AND ROUTING

REFERENCES

<table>
<thead>
<tr>
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</thead>
</table>
OBJECTIVES:
1. To study the concepts of CMOS and BICMOS analog circuits.
2. To understand the concepts of A/D converters and analog integrated sensors.
3. To understand the testing concepts in analog VLSI circuits and its statistical modelling.

OUTCOMES:
1. Students will be able to understand the concepts of analog design and to design various analog systems including data converters- CMOS amplifiers- A/D Conversion.

UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW-VOLTAGE SIGNAL PROCESSING
Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOS Transistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING & NEURAL INFORMATION PROCESSING
Continuous Time Signal Processing-Sampled-Data Signal Processing-Switched- Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNIT III SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS

UNIT IV DESIGN FOR TESTABILITY & ANALOG VLSI INTERCONNECTS

UNIT V STATISTICAL MODELING & SIMULATION, ANALOG-DIGITAL LAYOUT

REFERENCES

<table>
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<tr>
<th>S.NO</th>
<th>Author(s) Name</th>
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<td>Malcom R. Haskard, Lan C. May</td>
<td>Analog VLSI Design - NMOS and CMOS</td>
<td>Prentice Hall, New Jersey</td>
<td>1998</td>
</tr>
</tbody>
</table>
OBJECTIVE:
1. To understand the basic knowledge of Nanotechnology.
2. To study the various nano-scaled Device models.

OUTCOMES:

UNIT I INTRODUCTION TO NANOTECHNOLOGY

UNIT II ELECTRICAL RESISTANCE - AN ATOMICISTIC VIEW

UNIT III MOLECULAR ELECTRONIC DEVICES
Basic Concepts- Self assembled Layers, Charge transport Mechanisms; Synthesis of Molecular wires and devices – synthesis of two terminal devices, Fabrication of molecular transport devices; Simple SAM metal-insulator-metal Tunneling.

UNIT IV NANOSCALE DEVICE MODELING
Inadequacy of macroscopic models, Equilibrium, Non-Equilibrium, Density Matrix and current operator; NEGF Formalism – Broadening.

UNIT V NANOSCALE DEVICE MODELING
Quantum Point Contact- Hamiltonian, Self energy; SAM- Signals used to control and probe molecules, Synthesis; Fabrication and overview of Nanotube devices- their properties.

REFERENCES

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<td>Chris Binns</td>
<td>Introduction to Nano science and Nano Technology</td>
<td>John wiley &amp; sons</td>
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</tr>
</tbody>
</table>
OBJECTIVE:
1. To study the concepts of random access memory and nonvolatile memories.
2. To learn the implementation methods and problems in designing and making semiconductor memories.
3. To understand different fault modeling and testing techniques.

OUTCOMES:
The students will be able to
1. Design MOS memories.
2. Design memory fault modeling and memory design test-abilities.

UNIT I RANDOM ACCESS MEMORY TECHNOLOGIES

UNIT II NONVOLATILE MEMORIES
Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture

UNIT III MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE

UNIT IV SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS

UNIT V PACKAGING TECHNOLOGIES
(3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

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</table>
OBJECTIVE:
1. To introduce the physical design concepts such as routing, placement, partitioning and packaging and to study the performance of circuits layout designs, compaction techniques.

OUTCOMES:
1. To know the basic VLSI design configurations

UNIT I INTRODUCTION TO VLSI TECHNOLOGY
Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies-Packaging-Computational Complexity-Algorithmic Paradigms

UNIT II PLACEMENT USING TOP-DOWN APPROACH

UNIT III ROUTING USING TOP DOWN APPROACH

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT

UNIT V SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION

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<td>Ban Wong, Anurag Mittal, Yu Cao, Greg Starr</td>
<td>Nano CMOS Circuit and Physical Design</td>
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<td>Naveed A. Sherwani</td>
<td>Algorithm for VLSI Physical Design Automation</td>
<td>Springer</td>
<td>1998</td>
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</table>
OBJECTIVES:
1. To learn the importance and issues in the design of RF
2. To design RF filter and RF antennas

OUTCOMES:

UNIT I  SWITCHING
RF MEMS relays and switches: Switch parameters, Actuation mechanisms, Bistable relays and micro actuators, Dynamics of switching operation.

UNIT II  COMPONENTS - I
MEMS inductors and capacitors: Micro machined inductor, Effect of inductor layout, Modeling and design issues of planar inductor, Gap tuning and area tuning capacitors, Dielectric tunable capacitors.

UNIT III  COMPONENTS - II
MEMS phase shifters: Types. Limitations, Switched delay lines, Micro machined transmission lines, coplanar lines, Micro machined directional coupler and mixer.

UNIT IV  FILTERS

UNIT V  ANTENNAS
Micro machined antennas: Microstrip antennas – design parameters, Micromachining to improve performance, Reconfigurable antennas.

TEXT BOOKS

<table>
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<tr>
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<td>H.J.Delos Santos</td>
<td>RF MEMS circuit Design for Wireless Communications</td>
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<td>3</td>
<td>G.M.Rebeiz</td>
<td>RF MEMS Theory, Design and Technology</td>
<td>John Wiley</td>
<td>2003</td>
</tr>
</tbody>
</table>
OBJECTIVES:
1. To introduce concepts related to Electromagnetic interference in PCBs.
2. To teach solutions for minimizing EMI in PCBs.
3. To teach EMI standards in the design of PCBs.

OUTCOMES:
1. Ability to analyze Electromagnetic interference effects in PCBs.
2. Ability to propose solutions for minimizing EMI in PCBs.

UNIT I EMI/EMC CONCEPTS
EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES
Conducted, radiated and transient coupling; Common ground impedance coupling; Common mode and ground loop coupling; Differential mode coupling; near field cable to cable coupling, cross talk; Field to cable coupling; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES
Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV EMC DESIGN OF PCBs
Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

UNIT V EMI MEASUREMENTS AND STANDARDS
Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx/Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL-461E/462.

REFERENCES

<table>
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<tr>
<th>S.NO</th>
<th>Author(s) Name</th>
<th>Title of the book</th>
<th>Publisher</th>
<th>Year of publication</th>
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<tbody>
<tr>
<td>3</td>
<td>Bernhard Keiser</td>
<td>Principles of Electromagnetic Compatibility</td>
<td>Artech house, Norwood</td>
<td>1987</td>
</tr>
</tbody>
</table>
OBJECTIVES:
1. To study the basic concepts of speech signal processing.
2. To study the analysis of various filter speech processing.
3. To learn various transform coders for audio coding.
4. To study the speech processing methods in time and frequency domain

UNIT I MECHANICS OF SPEECH

UNIT II TIME DOMAIN METHODS FOR SPEECH PROCESSING

UNIT III FREQUENCY DOMAIN METHOD FOR SPEECH PROCESSING
Short Time Fourier analysis – Filter bank analysis – Formant extraction – Pitch Extraction – Analysis by Synthesis- Analysis synthesis systems- Phase Vocoder—Channel Vocoder.
HOMOMORPHIC SPEECH ANALYSIS

UNIT IV LINEAR PREDICTIVE ANALYSIS OF SPEECH

UNIT V APPLICATION OF SPEECH SIGNAL PROCESSING

REFERENCES

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>1</td>
<td>Ben Gold and Nelson Morgan</td>
<td>Speech and Audio Signal Processing</td>
<td>John Wiley and Sons Inc. Singapore</td>
<td>2004</td>
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<tr>
<td>3</td>
<td>Quatieri</td>
<td>Discrete-time Speech Signal Processing</td>
<td>Prentice Hall, New Jersey</td>
<td>2001</td>
</tr>
</tbody>
</table>
15MEVL_E16 DSP PROCESSOR ARCHITECTURE AND PROGRAMMING

UNIT I FUNDAMENTALS OF PROGRAMMABLE DSPs
Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in P- DSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

UNIT II TMS320C5X PROCESSOR
Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

UNIT III TMS320C3X PROCESSOR
Architecture – Data formats - Addressing modes – Groups of addressing modes- Instruction sets - Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals – Generating and finding the sum of series, Convolution of two sequences, Filter design

UNIT IV ADSP PROCESSORS
Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

UNIT V ADVANCED PROCESSORS

REFERENCES

<table>
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<tr>
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</thead>
</table>
UNIT I SYMMETRIC CIPHERS

UNIT II PUBLIC-KEY ENCRYPTION AND HASH FUNCTIONS

UNIT III NETWORK SECURITY PRACTICE

UNIT IV SYSTEM SECURITY

UNIT V WIRELESS SECURITY

REFERENCES

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<tr>
<td>3</td>
<td>Bruce Schneier</td>
<td>Applied Cryptography</td>
<td>John Wiley and Sons Inc</td>
<td>2001</td>
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<td>5</td>
<td>Charles B. Pfleeger,</td>
<td>Security In Computing</td>
<td>Pearson Education</td>
<td>2003</td>
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<td></td>
<td>Shari Lawrence Pfleeger</td>
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</table>
OBJECTIVES:
1. To learn in detail about fabrication process.
2. To learn in detail about packaging of VLSI devices.

OUTCOMES:
1. To know the basic VLSI design technology

UNIT I CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION
Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

UNIT II LITHOGRAPHY AND RELATIVE PLASMA ETCHING
Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments,

UNIT III DEPOSITION, DIFFUSION, ION IMPLEMENTATION AND METALISATION

UNIT IV PROCESS SIMULATION AND VLSI PROCESS INTEGRATION.

UNIT V ANALYTICAL, ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES

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<td>S.M.Sze</td>
<td>VLSI Technology</td>
<td>McGraw-Hill</td>
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<td>2</td>
<td>Amar mukherjee</td>
<td>Introduction to NMOS and CMOS VLSI System design</td>
<td>Prentice Hall India</td>
<td>2000</td>
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<td>3</td>
<td>James D Plummer, Michael D. Deal, Peter B.Griffin</td>
<td>Silicon VLSI Technology: fundamentals practice and Modeling</td>
<td>Prentice Hall India</td>
<td>2000</td>
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<td>4</td>
<td>Wai Kai Chen</td>
<td>VLSI Technology</td>
<td>CRC press</td>
<td>2003</td>
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</tbody>
</table>
OBJECTIVES:
1. To expose the students to the fundamentals of microprocessor architecture.
2. To introduce the advanced features in microprocessors and microcontrollers.
3. To enable the students to understand various microcontroller architectures.

OUTCOMES:
1. The student will be able to work with suitable microprocessor / microcontroller for a specific real world application.

UNIT I MICROPROCESSOR ARCHITECTURE

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE: ARM

UNIT IV MOTOROLA 68HC11 MICROCONTROLLERS

UNIT V PIC MICRO CONTROLLER
CPU architecture – Instruction set – Interrupts – Timers – I/O port expansion –I2C bus for peripheral chip access – A/D converter – UART

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<tr>
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<td>James L. Antonakos</td>
<td>The Pentium Microprocessor</td>
<td>Pearson Education, New Delhi</td>
<td>1997</td>
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<td>3</td>
<td>Steve Furber</td>
<td>ARM System –On –Chip architecture</td>
<td>Addison Wesley, New Jersey</td>
<td>2000,</td>
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OBJECTIVE:
1. To know about CMOS circuit characteristics and their performance.
2. To understand the working of major building blocks (adders, multipliers, RAMs, and ROMs)
3. To clocks and power distribution networks.

OUTCOMES:
On successful completion of this course, students will be able to
1. know basics of VLSI design fundamentals
2. know various mathematical approaches for designing
3. study the performance of CMOS circuits
4. to design complex VLSI circuits
5. to design low power systems

UNIT – I  MOS TRANSISTOR THEORY

UNIT – II  CMOS PROCESSING TECHNOLOGY

UNIT – III  CIRCUIT CHARACTERISTICS & PERFORMANCE ESTIMATION

UNIT – IV  CMOS CIRCUIT AND LOGIC DESIGN

UNIT – V  CMOS SUBSYSTEM DESIGN

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<td>Principles of CMOS VLSI</td>
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<td>Neil H. E. Weste and K. Eshragian</td>
<td>Design</td>
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<td>3</td>
<td>Jacob Baker R., Harry W. Li, &amp; David K. Boyce</td>
<td>CMOS Circuit Design</td>
<td>PHI, New Delhi</td>
<td>2000</td>
</tr>
</tbody>
</table>
VALUE ADDED COURSES

15MEVA*51 CADENCE TOOL  2 0 0 2 100
Introduction to Cadence – Digital circuit design – Analog circuit design – Build gates – verilog XL – Simulation and timing – Comparison of simulators – Cell design

15MEVA*51 MATLAB PROGRAMMING  2 0 0 2 100
UNIT - I INTRODUCTION TO MATLAB

UNIT – II SIGNAL AND IMAGE PROCESSING TOOLBOX FUNCTION

15MEVA*51 STRATEGIES FOR ARTICLE WRITING AND PUBLISHING  2 0 0 2 100
PART I STAGES IN WRITING ARTICLES
Original research topic – novel approach to problems – concentrating on one or two fields – generating one or two papers from projects/thesis – critical thinking – working abstracts – eye-catching title - splitting different ideas in different papers – keeping it brief – depth in the approach - main assumptions and results - importance of introduction and conclusion – making the content interesting – no plagiarism – mentioning important references – preparing a blue print - definition of symbols used – source citations acknowledgements – confidentiality of the articles.

PART II JOURNAL PUBLICATION
Understanding research ethics and academic integrity – motivation to publish – difference in the approach between conference publishing and publishing in articles – search current journals – e-journals – finding the most appropriate journals - peer review process – difference between the ISBN & ISSN – the impact factor – formatting as required by journals – rankings for sole author / co-author(s) - cover page – cover letter – rejection and revision – responding to comments from referees – resubmission – quality not quantity of journals.